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Flipping Over Flip-Chip

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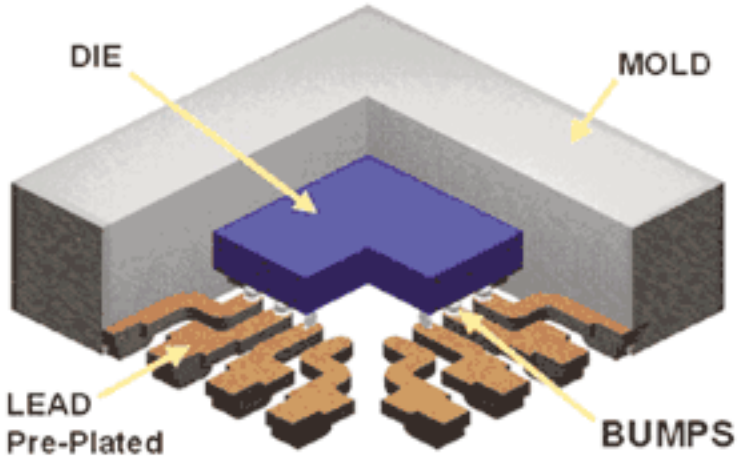
Today, the electronics industry is demanding higher density, faster speed, improved thermal performance and lower-cost packaging options. The flip-chip package is the answer to these requirements.

Up until now, the use of the wire-bonding technique has been a fundamental process in the packaging of ICs. However, as IC technology migrates toward 0.13-micron process geometries, requiring pin-counts greater than 1,000 and surpassing 20 watts, the wire-bonded package is no longer feasible.

Flip-chip packaging utilizes a technique to "bump" the wafer using high-lead solder, or eutectic solder, then "flips" the chip over in order to make the connection to the substrate/lead frame. By using this technique, the flip-chip can provide flexibility in order to redistribute the bond pad in an array format, enabling greater I/O counts. The bumping process relies on under bump metal (UBM) to redistribute the I/O, then uses various methods to apply the bump materials on the UBM, including screen-printing, rack plating and fountain plating.

For the high-end processors, graphics and networking devices, the high-performance flip-chip (FCBGA) provides an ideal solution. The package configuration is comprised of a flip-chip directly attached to the substrate with an underfill material supporting the coefficient of thermal expansion (CTE) mismatch between the silicon and the organic substrate. Because this package has two direct thermal paths for heat dissipation, it offers the best thermal performance package currently available in the market.



QFN

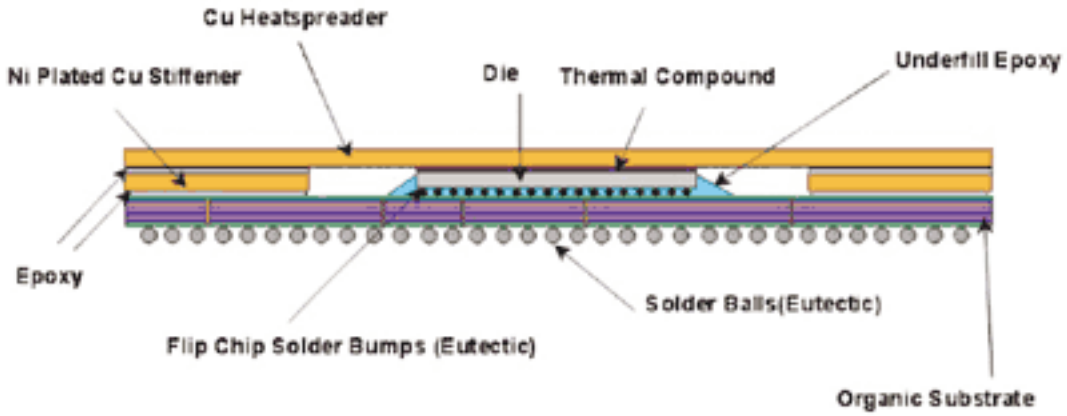
The second feature of the FCBGA package performance is in the substrate technology, where a high-routing density substrate is needed to route out the inner bump rows. One option is the 3M Microlam substrate, which is currently leading the high-density arena by offering seven layers of fine geometry for the 20-micron trace and 30-micron space width. A more commonly used high-density substrate is the Build-Up substrate, which uses a core layer and "build up" of 6 to 10 layers.

For the low lead-count (less than 200 I/O) packages, the flip-chip package can also be applied to a BGA or lead-frame package. The low lead-count BGAs are widely used in the fine-pitch (FPBGA) and chip-scale package (CSP) assembly processes. This package uses a two-layer BT substrate similar to the wire-bond FPBGA package, and the outline is the same, covering ball pitches ranging from 0.5mm to 1.0mm. It is possible for the FCBGA package to reduce the footprint by eliminating the required space for wire bonding on some of the designs. This package is ideal for high-frequency applications including portable and handheld electronic devices.

Cost and high-volume production capabilities are crucial in the development of flip-chip packaging technologies. In cases where the pin-count is less than 100

I/O and body size ranges from 3mm by 3mm to 10mm by 10mm, a very thin quad flat package no leads (VQFN) type of package is used for the flip-chip application. This reduces the inductance value by 40 percent when compared to a wire-bond package with a 3mm-by-3mm body size and makes it is suitable for any application with a low inductance requirement. The assembly process for this package enables the required low-cost and high-volume production of the flip-chip package.

High-lead and eutectic solder bump material can also be used for this process, and Advanpack Solutions PTE Ltd. (APS) of Singapore has developed a new bumping process that uses a copper pillar as a standoff and solder paste on the tip to connect it to the lead frame. An advantage of this process is the copper pillar's high standoff of 100 micron—which enables better flow for the overmold compound. In addition, since the pillar is copper with the solder paste away from the die, the alpha emissions are greatly reduced.



FCBGA

Today, flip-chip technology is widely used in many high-performance applications to meet the demands of the electronics industry for higher density, faster speed and improved thermal performance packaging solutions. Various package configurations have been developed to meet these requirements, including the high-performance BGA and the flip-chip FPBGA. In addition, the flip-chip on lead-frame package meets the market demand for a low-cost and high-performance solution for low lead-count applications. As the packaging requirements of the electronic industry evolve and process geometries become finer, flip-chip technology will continue to adapt in order to provide the best solution for low to high I/O count applications.

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