ADVANCED CONNECTIONS

Advanced Interconnect Technologies | Spring 2002

AIT 2002 Outlook

Ralph Duceour
President and CEO

The year 2001 marked one of the worst downturns in the history of the semiconductor industry. In response to this challenging market, AIT has focused aggressively on internal cost reduction and reorganized its internal work force to improve efficiencies. The company has also expanded its capabilities with the development of new packaging technologies, acquisitions, and the addition of key personnel to help strengthen AIT's global leadership in assembly and test services.

In the past year, AIT grew its assembly and test services capabilities with the acquisition of two U.S. based test facilities; Multitech Design & Test Labs (MDT) based in Sunnyvale, Calif. and Semiconductor Services, based in Austin, Tex. Both acquisitions were completed in the second quarter of 2001. The addition of these two companies has enabled AIT to extend programs in production test services and test program software development.

During the fourth quarter AIT signed licensing agreements with LSI Logic, based in Milpitas, Calif. and Advanpack Solutions PTE. Ltd. of Singapore that provide the company with the rights to assemble two unique advanced flip-chip semiconductor packaging technologies. These licensing agreements provide strong additions to the AIT technology portfolio and make the company one of the industry's most advanced technology providers in the high-growth, flip-chip packaging segment.

Continuing to build a strong executive management team, AIT appointed George A. Shaw Jr. as senior vice president of operations, Hong Kong; Wayne F. Moore as vice president of sales, strategic accounts; and Clyde R. Hosein as senior vice president, finance and administration and chief financial officer (CFO) during 2001.

Overseas at AIT's Hong Kong facility, restructuring of the factory continued with the establishment of full service test and production volume wafer probe capabilities on the 6th floor. In the fourth quarter, upon finalization of the LSI flip-chip technology license agreement, capital investments were made to purchase and install flip-chip assembly equipment.

In Batam, the transfer of all leaded packages from the Hong Kong facility was completed during 2001. Additional package configurations, including VFQFP-N and flip-chip were added to support new customer needs in existing leaded and non-leaded package products. Numerous cost reduction projects were completed during 2001 including areas such as materials cost, assembly techniques and freight costs.

AIT's management and ownership is committed to strengthening its position as a global supplier of semiconductor assembly and test services, and continuing to offer leading technology and manufacturing solutions to its customers. AIT will continue to focus on cost reduction in order to remain financially sound and debt-free in 2002. The company will continue to strengthen the internal organizational structure by adding seasoned management and personnel to support the future growth of the company. AIT will also continue to pursue strategic acquisitions and execute capital expenditures required to remain competitive in the market and provide exceptional customer service, while meeting market demands for rapid product introduction and production ramp.

Yours Sincerely,

Ralph Duceour

INSIDE

2 .... Technology
3 .... Development
5 .... Factory News
6 .... Environment
7 .... Expansion
8 .... New to AIT

TECHNOLOGY

AIT Inks Flip-Chip Licensing Agreements with LSI Logic and Advanpack Solutions

Reinforcing its commitment to providing advanced packaging solutions for a variety of end-use applications, including mobile phones, notebook computers and networking systems, AIT recently signed separate flip-chip packaging licensing agreements with LSI Logic Corporation and Advanpack Solutions PTE, Ltd. (APS). The addition of the flip-chip package will broaden AIT's current offering of array packaging solutions which already includes plastic ball grid array (PBGA), fine pitch ball grid array (FBGA), flex ball grid array (FxBGA), Tape BGA (TBGA) and enhanced ball grid array (EPBGA) varieties.

In October 2001, AIT entered into an agreement with LSI Logic to license the company's organic laminate flip chip (FC BGA) technology. Based in Milpitas, Calif., LSI Logic is a leading designer and manufacturer of communications, consumer and storage semiconductors for applications that access, interconnect and store data, voice and video.

LSI Logic's flip chip ball grid array (FC BGA) packaging technology offers an advanced solution for high performance ASIC and system-on-a-chip (SoC) designs. The FC BGA is ideal for use in broadband, networking, computing and storage applications.

The licensing agreement with LSI Logic provides AIT access to LSI Logic's FCBGA-HP (high performance) package technology. (see figure 1)

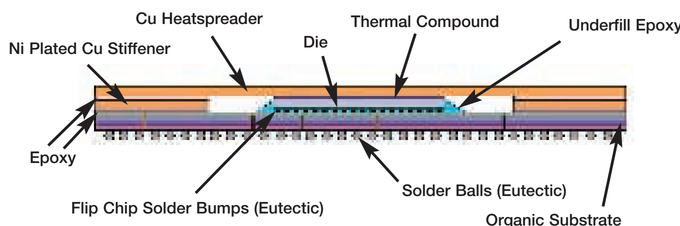


figure 1 – FCBGA-HP (high performance) package

The agreement also includes assembly processes and materials, qualification of each substrate type, the use of LSI Logic's standard package offerings and the characterization data of standard packages.

"With this agreement, AIT now has access to the semiconductor industry's most advanced flip-chip packaging technology. This is important because we're seeing increased demand for this technology from our customers in the telecommunications, computing, and storage applications markets," said Ralph Duceour, president and CEO of AIT. "The agreement extends our technology portfolio to encompass a full-range of offerings from high-volume leaded packages to cutting-edge flip chip solutions."

AIT's LSI Logic flip chip development began in Q4' 01 with the FCBGA-HP. AIT completed line certification for the LSI Logic FCBGA-HP in January 2002, and production of the organic substrates will begin upon completion of package qualification.

In addition to the licensing agreement with LSI Logic, AIT signed an agreement with APS in November 2001, further enhancing the company's flip-chip capabilities, and providing AIT with the rights to assemble proprietary pillar-bumped, flip-chip semiconductor packages. Based in Singapore, APS is a provider of advanced flip-chip packaging solutions and wafer-level packaging for communications applications including data networking, broadband and wireless communications. (see figure 2)

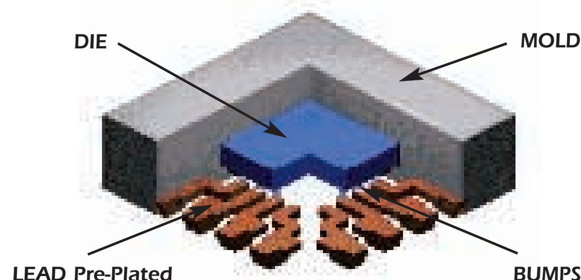


figure 2 – Flip Chip VFQFP-N package

Pillar bumped packages are essential for small-footprint semiconductors required in cellular telecommunications (phones and pagers), PCMCIA cards, memory cards, digital cameras and camcorders. This agreement, coupled with AIT's recent licensing of LSI Logic's organic flip-chip FC BGA technology, reinforces the company's commitment to provide the industry's most advanced flip-chip packaging solutions.

"This agreement with APS provides us with access to a low-cost, flip-chip assembly technology that is critical to the development of low and mid-range lead-frame products that have traditionally been served by wire bonding packages," continued Duceour. "This licensing agreement is a strong addition to our technology portfolio and makes us one of the industry's most advanced technology providers in the high-growth, flip-chip packaging segment."

APS's unique pillar bumping interconnect technology, (see figure 3) uses perimeter or array flip-chip pads to connect an integrated circuit (IC) to a copper lead frame. Pillar-bumped flip-chip packages provide superior electrical and thermal enhancement and a lower profile than available with current wire bond technology. The small size and reduced weight, along with excellent thermal and electrical performance, make the packages an ideal choice for portable and handheld products.

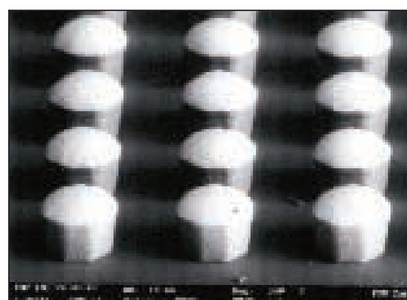


figure 3 – APS Pillar Bump Technology

The applications for this package range from RF and analog, power devices, memory, and communications devices which all benefit from the lower cost structure and small form factor achieved with the APS flip chip package solution. APS's package technology offers a "lead free" option for customers who need to meet the demand for "green technologies" today.

By signing these separate agreements with LSI Logic and APS, AIT is well positioned to provide its customers with leading-edge flip-chip packaging solutions now and in the future.

PACKAGE DEVELOPMENT

AIT Develops VFQFP-N and WFQFP-N Packages

In response to customer requests for small-outline packages that combine the performance benefits of an array package with the cost-competitiveness of a lead-frame package, AIT will begin production of wire bond and flip chip configurations of its Very Thin Fine Pitch Quad Flat Packages – No Leads (VFQFP-N) and Very Very Thin Fine Pitch Quad Flat Packages – No Leads (WFQFP-N) in 2002. The small size of these packages, coupled with excellent thermal and electrical performance, makes the VFQFP-N and WFQFP-N packages ideal for handheld and portable communications applications including cellular phones, personal digital assistants (PDAs) and other applications where small, high performance packages are required.

AIT's VFQFP-N and WFQFP-N are performance and efficiency competitive with today's array packages including the FBGA because they to do not use BGA substrates, and do not require expensive ball tooling thus providing a better cost solution. The VFQFP-N and WFQFP-N can be used as alternatives to low lead count array packages as well as leaded packages such as SOICs, MMCs and TSSOP packages.

The VFQFP-N and WFQFP-N also possess certain mechanical advantages including improved co-planarity and heat dissipation. The electrical performance of the packages is superior to traditional leaded packages because the VFQFP-N and WFQFP-N do not have gull wing leads which can sometimes act as antennas, creating "noise" in high-frequency applications. In addition, the package also provides excellent thermal performance through the exposed lead-frame pad, which enables a direct thermal path for removing heat from the package. This thermal enhancing feature can be further taken advantage of when the package lead-frame pad is soldered to the board.

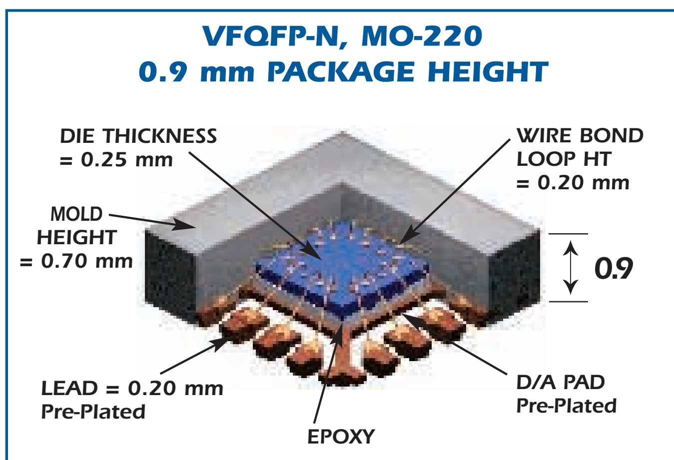
AIT is currently in the process of completing the internal qualification of the VFQFP-N and WFQFP-N packages and will complete the customer qualification of the packages in Q2'02. Production is scheduled to begin in Q3'02. The VFQFP-N and WFQFP-N will be manufactured at AIT's factory in Batam.

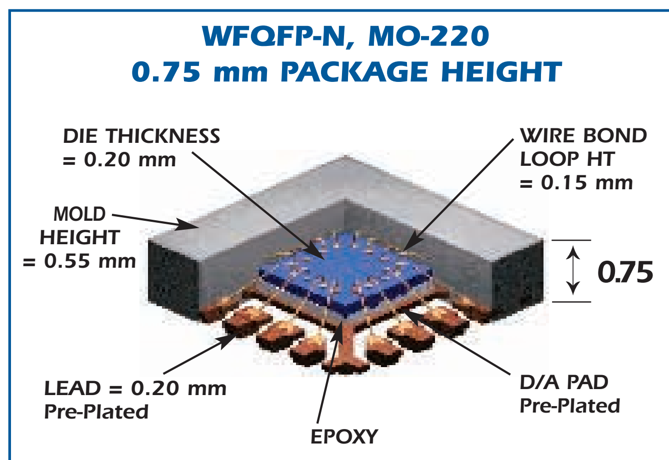
The VFQFP-N and WFQFP-N will be manufactured using four mold blocks of matrix array packages (MAP) on a fixed lead frame outline to produce more than five times the density of traditional matrix lead frames. The use of pre-plated (PPF) lead frames will eliminate the optional solder plating, and the laser marked identity on each strip will enable the Auto-line to download process instructions for device laser mark, saw streets and offload for the blinded MAP device(s). Because the VFQFP-N and WFQFP-N packages will be manufactured using the MAP mold blocks on the lead-frame, they will not require the amount of custom tooling typically needed in the production of array packaging devices, ultimately lowering the cost of the finished product.

To reduce cycle time, improve time-to-market and cost efficiencies, AIT has implemented several steps in the manufacturing process, including a program that will enable the activities of each transaction across the Auto-line to be supervised by CELL Controllers, connected to the factory HOST. This will result in paper-less processing, real-time customer visibility and closed-loop compliance. In addition, AIT will also utilize a universal and common lead frame design with the laser marked identification of each strip enabling the factory HOST to guide the Auto-lines. Through this process, a CELL controller links the HOST in to handle a "line" and the HOST controls multiple "lines" providing a way to track WIP and QC data efficiently. Advantages of this new process include a machine to man ratio of 1:1, fully modular packages for easy expansion and integration, and auto-logistics to maximize utilization.

AIT DEVELOPS CONTINUED ON PAGE 4 . . . . . .

diagram 1: Cross Section of the Wire Bond VFQFP-N and WFQFP-N Packages.





PACKAGE DEVELOPMENT

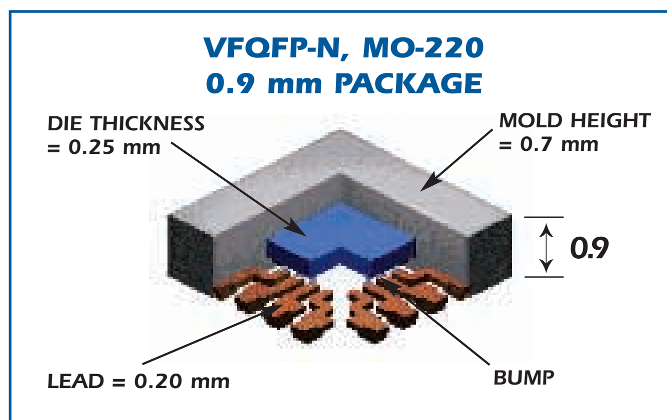
AIT DEVELOPS CONTINUED FROM PAGE 3. . . . .

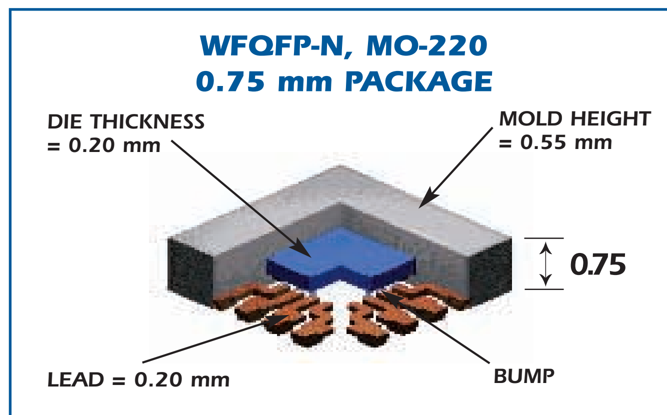
The wire bond version VFQFP-N and WFQFP-N will be offered in the following sizes and lead counts:

Body Size (mm)	Lead Count	Die Pad (mm^2)	Maximum Die Size – without ground (mm^2)	Maximum Die Size – with ground (mm^2)
2 x 2	8	0.8	0.55	–
3 x 3	4, 8, 12, 16	1.5	1.25	0.74
4 x 4	12, 16, 20, 24	2.5	2.25	1.74
5 x 5	20, 24, 28, 32	3.5	3.25	2.74
6 x 6	20, 28, 36, 40	4.5	4.25	3.74
7 x 7	28, 32, 44, 48	5.0	4.75	4.24
8 x 8	32, 36, 40, 44, 48, 52, 56	6.5	6.25	5.74
9 x 9	44, 48, 56, 60, 64	7.75	7.5	7.0
10 x 10	64, 68, 76, 80	8.25	8.0	7.5
12 x 12	80	10.25	10.0	0.5
15 x 15	TBD	–	–	–

AIT recently licensed copper pillar bumping technology from Advanpack Solutions PTE, Ltd. (APS) of Singapore (see “Flip-Chip” pg. 2). The pillar bumping process offers a number of advantages over the current solder bump and gold bumping. These include the absence of silver spot plating or “dimple” on the copper lead frame; no requirements for special finishing treatment on the lead frame; the elimination of “uncontrolled volume” solder paste printer on the lead frame, the die tilt, and the solder wicking/flow out during molding. Additional advantages include a shorter manufacturing cycle and the ability to choose the metallurgy tip whether it be silver epoxy, lead-free or eutectic solder. The pillar bump has copper posts that are a minimum of 100µm in length. Unlike the solder and gold bumps, the pillar bump has a high profile attachment, better coplanarity and ease of mold flow under the die.

diagram 2: Cross Section of the Flip-Chip VFQFP-N and WFQFP-N Packages.





Flip-Chip VFQFP-N and WFQFP-N offering:

Body Size (mm)	Lead Count	Minimum Bump Pitch	Standard Bump Height
2 x 2	8		
3 x 3	4, 8, 12, 16		
4 x 4	12, 16, 20, 24		
5 x 5	20, 24, 28, 32		
6 x 6	20, 28, 36, 40	200µm	100µm
7 x 7	28, 32, 44, 48		
8 x 8	32, 36, 40, 44, 48, 52, 56		
9 x 9	44, 48, 56, 60, 64		
10 x 10	64, 68, 76, 80		
12 x 12	80		
15 x 15	TBD		

The VFQFP-N and WFQFP-N are compliant with the JEDEC standard MO-220 outline.

* Flip-chip will be offered initially in 3 x 3, 4 x 4, 5 x 5 and 7 x 7 formats using copper pillar bumps licensed from Advanpack Solutions PTE, Ltd. (APS) of Singapore.

* Contact AIT Marketing for Non-standard bump requirement.

* Basic lead time for non-existing package offering: lead frame – 4 weeks, saw jigs – 6 weeks.

FACTORY NEWS

AIT Hong Kong Update

AIT's Hong Kong facility underwent several changes in 2001 in order to enhance the range of assembly and test services for its array packaging customers.

AIT's thermal measurement lab was established in June 2001 and the electrical lab was completed in Dec. 2001. By setting up a thermal/electrical lab at the Hong Kong factory, AIT can prepare measurement samples of the thermal/electrical performance on-site, enabling the characterization team to work closely with the design team. The purpose of the thermal/electrical measurement lab is to provide accurate electronic package thermal and electrical performance data to the customer using reliable measurement methodologies. By measuring the effects of various package parameters, the thermal/electrical lab can provide the guidelines for the design and development of packaging technologies.

Second-level board testing at AIT's Hong Kong facility began in July 2001. By adding second-level board testing, AIT can determine and assess solder joint reliability performance when the package is mounted on a printed circuit board (PCB). Second-level board testing is applied to all surface mount packages.

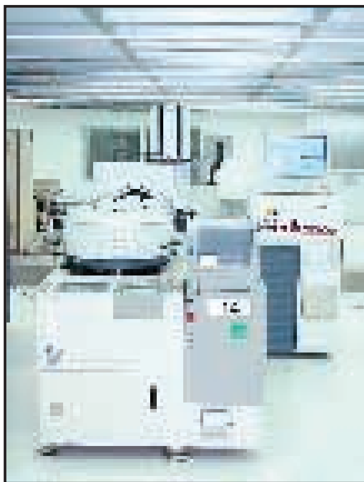


figure 1 – TSK A-PM-90A wafer prober

In Oct. 2001, the Hong Kong facility began providing wafer probing services. (see figure 1) The company added an SC Micro tester at 50 megahertz (MHz) with 256 I/O and 128 megabits (Mb) of scan memory and a TSK-90-A 6-inch/8-inch prober which is used with a GPIB interface with an inkless wafer map. The final package configurations of a probed device include two 35 square millimeter (mm2) 313 ball plastic ball grid array (PBGA) packages in 6-inch and 8-inch wafers.

In Dec. 2001, AIT's Hong Kong factory completed the transfer of leaded package production to the Batam factory. As a result, AIT Hong Kong is now focused on the development of array and high-end packaging technologies. The areas that were formerly set aside for leaded assembly are being re-tooled to accommodate the assembly of new and emerging ball grid array (BGA) technologies including flip chip and System-in-Package (SIP).

AIT commenced the lead-free process qualification of the PBGA and FBGA packages. The lead-free process for PBGA is scheduled for completion in Q1'02, and the process for FBGA is expected to be final in Q2'02. The benefits of the lead-free PBGA and FBGA packaging process for AIT's customers include environmental friendliness (no lead waste); higher reliability; and compliance with the requirements of the United States Environmental Protection Agency (EPA) and the European Commission on Electrical and Electronic Waste Directive.

AIT's Hong Kong facility also achieved ISO14000 and ISO9000:2000 certification in Sept. 2001. The Hong Kong facility was the first AIT factory to receive the ISO9000:2000 certification. The qualification process for each of these certifications took place over a 9 to 12 month period and the certificate remains in effect for three years.

In the fourth quarter of 2001, the LSI flip-chip technology licensing agreement was completed and capital investments were made at the Hong Kong facility to purchase and install flip-chip assembly equipment. The new equipment purchased includes a Disco DFD-651 dual spindle saw, a Datacon 2220 APM flip chip boner, a Heller 1800 EXL forced convection oven, an Asymtek M2020 underfill dispenser, a Dimos drawer type batch oven and a GPD Micromax adhesive dispensing and stiffener/heatspreader attach. This line has already been installed and certified by LSI. (see figure 2) The line is expected to be fully qualified by LSI in Q2'02. AIT began phase one of the flip chip process with the development of organic substrates including the FCBGA HP and FCBGA CSP in Q3'01. Production of the organic flip-chip substrates is slated for Q3'02. Phase two of the flip-chip development cycle that will include flex substrates is scheduled to begin in Q2'02, with production slated for 2003.

figure 2 – Hong Kong's Flip Chip Assembly Line

During 2002, AIT's Hong Kong facility will continue to offer one of the industry's broadest families of array packaging technologies. Through aggressive development, production and assembly of existing and emerging packages, AIT is positioned to capture a greater portion of the advanced packaging market.

ENVIRONMENT

Batam Lead-Free Update: "Green" Packaging Made Possible with Pure Tin

After extensive testing, AIT's Batam facility has concluded that pure tin is the ideal "drop-in" replacement for tin lead in leaded package surface finishing. The evaluation conducted at the Batam facility proved that after materials were stored at room temperature for 18 months with an accelerated test of 50 degrees Celsius for 13 months, no whisker growth was present. By eliminating whisker growth, short-circuiting of the devices during storage can be prevented.

In July 2001, AIT began working with a leading contract board manufacturer to conduct second level reliability testing for pure tin. Studies continue at the board assembly level in order to define the suitable re-flow temperature after considering various types of soldering paste and PCB finishing products for pure tin.

Why Pure Tin?

- Pure tin is a known process that has been used for years in the development of interconnection and integrated circuit (IC) products.
- Pure tin is easier to control during the manufacturing process because the parameters are smaller than those required by a tin-lead (Sn-Pb) compound.
- Pure tin is cost competitive with the existing Sn-Pb compounds.
- Processing for pure tin has improved due to a modification to the chemistry that suppresses whisker growth. Whisker growth not only affects pure tin, but also other tin-based alloys.
- Pure tin does not require any major modifications to the existing MECO solder plating lines.
- Pure tin enables an improved process for the treatment of waste water.
- Pure tin has broader based support from chemical suppliers.
- Because generic chemicals, with the exception of the additive system are used in the development of pure tin, there are no logistics issues.
- Pure tin is compatible with tin-based lead free solder pastes.

In August 2001, AIT Batam presented the results of its lead-free program at the Microelectronics Packaging and Test Engineering Council (MEPTEC) Lead-Free Summit in San Jose, Calif. The focus of the presentation was on the implementation of the lead-free solder and the adoption of pure tin as a drop-in replacement for the tin lead chemistry in Batam.

The acceptance of pure tin by the Lead-Free Summit attendees was overwhelming. Currently, whisker growth is the primary issue since no standard test method is available to determine if whisker growth exists. The definition and standard methods of whisker growth testing are expected to be released by the National Electronics Manufacturing Initiative (NEMI) Lead-Free Task Force within the next couple of months.

Testing

To support the implementation of pure tin as a drop-in replacement for tin lead, the following tests were conducted in Batam:

1. Physical/Mechanical Test: By examining the plating thickness, carbon content, ionic contamination, grain structure, lead fatigue and lead adhesion test, it was determined that the pure tin chemistry plated parts can comply with the industry standard and are comparable to tin lead plating.

2. Solderability Test: Pure tin successfully passed all of the solderability test conditions. The pre-conditioning of the parts included steam aging for 0, 8, 16 and 32 hours followed by a heat treatment at 150 degrees Celsius for 24, 48 and 96 hours. The solderability test utilized the "Dip and Look" test (Mil Std 883E method 2003.7), "Wetting Balance" test (Mil Std 883E method 2022.2), and Infrared (IR) Reflow Test (JEDEC B102-C). Sn-Ag-Cu solder pot and solder pastes were used for the evaluations.

3. Whisker growth test: The test was accelerated by storing the parts inside the oven at 50 degrees Celsius over a 14-month period. At the conclusion of the test no whisker was observed. The test also included storage of the parts at room temperature for a period of 18 months. Again, at the conclusion of the test, no whisker was observed. When storing the parts at 85 degrees Celsius (°C) with an 85 percent room humidity for 1000 hours, no whisker growth was observed. Finally, when temperature cycling (-65 to 150 °C) took place for 1000 cycles, no whisker growth was observed.

Batam Factory

Implementation

To date, thirteen customers have sent qualification lots to be plated with the pure tin chemistry in order to perform their own board level assembly qualification testing.

BATAM UPDATE CONTINUED ON PAGE 7 . . . . . .

EXPANSION

AIT Expands Testing Capabilities in Sunnyvale and Austin

In an effort to better support its customer's requirements for more fully integrated test and assembly processes, AIT continues to broaden its portfolio with the addition of new state-of-the-art testing equipment at its Sunnyvale, Calif. and Austin, Tex. testing facilities. One of the key elements driving the need for more complex testing equipment and the integration of test and assembly services, is the changing face of packaging technology. Over the past few years, demand has shifted from the digital domain to the complex mixed-signal and radio frequency (RF) arena. As a result, packages have become more complicated and diverse, and the role of test has become an integral part of the manufacturing process.

In Sunnyvale, AIT purchased a J750 Integra tester from Teradyne in December 2001, and the delivery date is set for spring of 2002. The J750 is a small footprint, cost-effective digital testing system with the option of mixed-signal testing capabilities. (see figure 1) Because of these features, the J750 has become one of the industry's most sought-after test platforms. Delivering high levels of parallel test with up to

figure 1 - J750 Integra tester from Teradyne

1,024 digital tester channels, the J750 enables AIT to test devices with I/O counts ranging from 512 to 1,024 at speeds of up to 100 megahertz (MHz). The J750 tester will also give AIT the ability to run multi-site at the final test, reducing the test cost for the customer.

Multi-site testing is increasing in popularity due to its cost-effectiveness. Typically, the customer is charged a unit price for testing services. For example, if a tester costs $100 per hour and the throughput is 100 units per hour, the cost per unit is $1 running single insertion. By using a tester capable of multi-site testing, like the J750 tester, there are automatic handlers that can test up to eight units at a time, thus increasing the throughput by roughly a factor of four depending on the number of units. With a throughput of 400 units per hour, the cost would be $0.25 per unit.

A Teradyne Catalyst Test System will be moved to AIT's Austin facility in the spring of 2002. The Catalyst is a fully loaded system offering fully integrated analog and digital

figure 2 - Teradyne Catalyst Test System

instrumentation and mixed-signal/System-on-Chip (SoC) digital testing with data rates up to 400MHz. (see figure 2) The Catalyst System features accurate and precise measuring units, designed to test the DC and AC characteristics of SoC devices, full spectrum AC instrumentation and Flex-DSP. In addition, the Catalyst's parallel computer architecture is designed to reduce the overall test time, accelerating test development and high-volume production for integrated circuits housing complex digital, embedded memory and high-performance analog components. The Catalyst System will not only support AIT's customers in the Austin area with testing capabilities for these mixed signal circuits, but help AIT significantly reduce time-to-market.

As electronic devices continue to grow in complexity and require more advanced packaging technologies, the role of test is changing. With the purchase of new equipment like the Teradyne J750 and Catalyst systems AIT can create a turnkey program that meets the requirements of its customers for a fully-integrated test and assembly process.

BATAM UPDATE CONTINUED FROM PAGE 6 . . . . . .

Other "Green Compounds"

AIT Batam is also evaluating other "Green Compound" candidates including Hitachi and Nitto mold compounds, and Ablebond and Sumitomo die attach epoxies. The company is now in the process of reliability testing of these compounds. Currently, Exar is in the process of qualifying the Sumitomo USQ mold compound for its LQ/TQFP products. This qualification is scheduled for completion in March 2002. Through the reliability testing, various Moisture Sensitivity Levels (MSL) and IR reflow conditions are considered. Preliminary results were released in July 2001 and final results are expected in Q1'02.

For additional information on the AIT Batam lead-free programs please visit www.aitsales.com

Evaluation Reports and Data are available on request.

NEW TO AIT

Hosein, Shaw and Moore Join Executive Management Team

To ensure continued strong and effective leadership for future growth, AIT recently expanded its executive management team to include Clyde R. Hosein as corporate chief financial officer (CFO); George A. Shaw Jr. as senior vice president of operations, Hong Kong; and Wayne K. Moore as vice president of sales, strategic accounts.

Hosein joined AIT in November 2001 and reports to Ralph Duceour. Hosein's responsibilities include managing the company's financial operations as well as corporate finance, human resources, administration and information systems. Hosein will also play a key role in the company's strategic acquisitions and investor relations. Reporting to Hubert Meier, Shaw joined AIT in October 2001 and is responsible for heading operations at AIT's array packaging factory in Hong Kong. Moore also joined AIT in October 2001 and reports to Duceour. Moore's primary responsibility is targeting and securing accounts that are strategic to the long-term growth and success of AIT.

"We are delighted to add these industry veterans to AIT's management team. Clyde, George and Wayne bring valuable experience and contributions to the company, and are instrumental in driving and supporting AIT's ambitious business growth initiatives," stated Duceour. "These appointments will help us achieve our goal of becoming one of the top semiconductor sub-contractor suppliers worldwide. Each will play a key role in AIT's efforts to expand the company's subcontracting services for semiconductor packaging, assembly and test, as well as grow our business to achieve status as one of the top suppliers worldwide."

Hosein brings more than 20 years of financial management experience to the CFO position at AIT. Prior to joining AIT, Hosein served as CFO for Candescent Technologies Corp. (San Jose, Calif.). Hosein also held several financial management positions with IBM Corp. during his 15-years with the company, which included advisory systems analyst and senior financial analyst to manufacturing controller.

Prior to joining AIT, Shaw served as senior vice president of the South Asia operations for Amkor Technology. Shaw also served as president of Alphatec, U.S.A., an independent supplier of semiconductor manufacturing services. Shaw has also held management positions at Applied Magnetics, Aptix Corp. and National Semiconductor.

Moore has held several presidential-level positions in the electronics industry, prior to joining AIT. He was most recently president of Signetics High Tech., a semiconductor assembly and test provider. Moore has also served as president of ASAT.

Clyde R. Hosein

George A. Shaw Jr.

Wayne K. Moore

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